Abstract of Disclosure

A semiconductor memory device includes an advanced prefetching block for prefetching more bit data at once and effectively arranging the prefetched data so as to reduce an address access time of the semiconductor memory device. The semiconductor memory device having four pipelining latches for prefetching 4-bit data outputted from at least one bank in response to a start address of the 4-bit data and control signals includes a first data multiplexing unit, a second data multiplexing unit, a third order multiplexing unit and a forth order multiplexing unit.